In the Specification:

Background of the Invention: Please replace the second full paragraph of page 2 with the following:

In addition to these off-line testing methods, the present inventors have also recently developed methods of testing and fault tolerant operation of the programmable logic blocks and methods of testing the programmable interconnect resources during normal on-line operation of the FPGAs. These testing and operating methods are set out in detail in U.S. Patent [[No.]] Nos. 6,256,758, 6,550,030, 6,631,487, 6,474,761, and 6,530,049 ~~and in pending U.S. Application Nos. 09/405,958, 09/671,853, 09/406,219, and 09/611,449~~ . The full disclosures in ~~this patent and patent applications~~ these patents are also incorporated herein by reference.

Detailed Description of the Invention: Please replace the paragraph bridging pages 12 and 13 with the following:

In order to minimize the number of reconfigurations required during testing and therefore the total testing time, the FPGA resources within the self-testing area 16 are preferably configured to include several testing regions 19 ($Region_1$, $Region_2$, . . . $Region_n$) as shown in Figure 4. Necessarily each tester 19 includes at least a TPG 20, an ORA 22, and two groups of WUTs 24. Comparative testing of the interconnect resources within each tester 19 is conducted concurrently. The present preferred comparison-based on-line method of testing the programmable interconnect resources briefly described above including the fault model utilized and configuration of the self-testing area is described in detail for programmable interconnect resources in the above-referenced ~~pending U.S. Application No. 09/406,219~~ U.S. Patent No. 6,574,761 and in C. Stroud ET AL., *Built-In Self-Test of FPGA Interconnect,* PROC. INTN'L TEST CONF., at 404-411, 1998

incorporated herein by reference. As indicated above, the present preferred method may target permanent faults that exist in a newly manufactured FPGA device or which appear during the lifetime of the FPGA under test.

Abstract of the Disclosure: Please replace the Abstract with the following:

A method of identifying faulty programmable interconnect resources of a field programmable gate array (FPGA) may be carried out during manufacturing testing and/or during normal on-line operation. The FPGA resources are configured into a working area and a self-testing area. The working area maintains normal operation of the FPGA throughout on-line testing. ~~During manufacturing testing, the working area may be replaced with additional self-testing areas or the self-testing area extended to include the entire FPGA.~~ Within the self-testing area, programmable interconnect resources of the FPGA are grouped and comparatively tested for faults. Upon the detection of one or more faults within a group of programmable interconnect resources, the group of resources is subdivided for further comparative testing in order to minimize a region of the group of resources including the fault for each fault. Once the region of the group of resources which includes the fault is minimized, the wires within the minimized region are comparatively tested in order to determine which wire includes the faulty resource or resources. Once the wire which includes the faulty resource is determined, a variety of testing configurations may be utilized to identify the faulty resource within the wire. ~~After testing the programmable interconnect resources in the initial self-testing area, the FPGA is reconfigured such that a portion of the working area becomes a subsequent self-testing area and at least a portion of the initial self-testing area replaces that portion of the working area. In other words, the self-testing area roves around the FPGA repeating the steps of testing and reconfiguring until the entire FPGA has undergone testing and its faulty programmable interconnect resources identified.~~